Fundamental Reduction Systems
Examination

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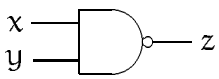
Tuesday, December 13, 1994, 14^{00}–16^{00}

The questions of this exam investigate the properties of some actual term rewrite systems meant to be useful in electronics. There are 11 questions (marked with a ▶ in the left margin) on 3 pages.

It is possible to model *electronic circuits* with reduction systems. In such a circuit, a number of logic-valued inputs are passed into a number of interconnected logic 'gates' that combine them in various ways to form some logic-valued outputs. We will denote logic values as 1 and 0 (for 'true' and 'false'), and will only consider one kind of logic gate, namely $\invamp$ (for 'inverted and'), usually called 'nand' and depicted



with truth table

x	y	z
0	0	1
0	1	1
1	0	1
1	1	0

(nand) (1)

implementing the logic function $z = x \invamp y \stackrel{\text{def}}{=} \neg(x \wedge y)$.

Definition 1. The term rewrite system *Nand* is intended to model the function of all possible nand-gate circuits with a single ouput. The terms are

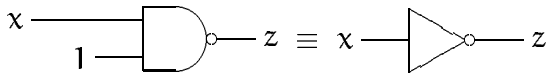
$$t \ ::= \ t \invamp t \ \mid \ 1 \ \mid \ 0 \tag{2}$$

and the rules

$$1 \invamp 1 \to 0 \tag{3}$$
$$0 \invamp x \to 1 \tag{4}$$
$$x \invamp 0 \to 1 \tag{5}$$

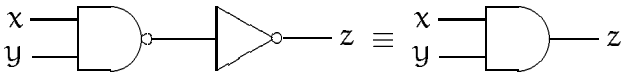
▶ **Question 1.** What are the normal forms?

► **Question 2.** Nand-gates can be used to model several other gates. Verify by reduction in the *Nand* system that each of the circuits given below in the left column behaves as the gate pictured in the middle with truth table to the right:



x	z
0	1
1	0

(inverter) (6)



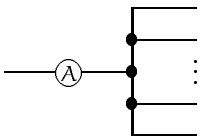
x	y	z
0	0	0
0	1	0
1	0	0
1	1	1

(and) (7)

► **Question 3.** Show that *Nand* is bounded.

► **Question 4.** Show that *Nand* is complete (*i.e.*, noetherian (SN) and confluent (CR)).

When building real circuits it is possible to connect a wire to more than one input and this is not captured by *Nand*. We will repair this by adding 'branching wire' components like



where crossing wires are connected when marked with •. We will only consider combinatoric circuits (without feed-back, *i.e.*, loops). Note that any such circuit corresponds to a *Nand*-circuit (without branching) by making a copy of the subcircuit generating the branched signal for each wire it is connected to.

Definition 2. The term rewrite system *NandC* is intended to model all combinatoric nand-gate circuits with a single ouput. The terms are as *Nand* with the addition of

$$t ::= @(t, t) \mid a \tag{8}$$

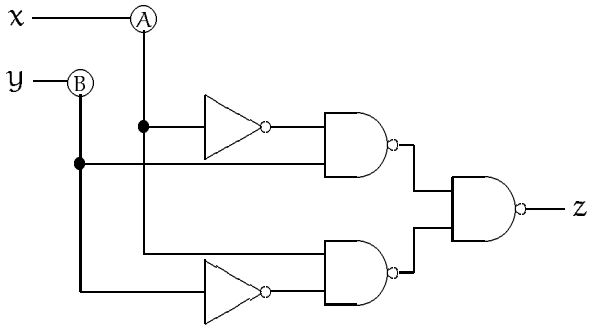
where a, b range over special 'branch constants' $A, B, \ldots$ of which we use as many as needed for each circuit, with the new rules

$$@(u, x \parr y) \to @(u, x) \parr @(u, y) \tag{9}$$
$$@(x, a) \to x \tag{10}$$
$$@(x, b) \to b \qquad \text{if } a \neq b \tag{11}$$
$$@(x, 0) \to 0 \tag{12}$$
$$@(x, 1) \to 1 \tag{13}$$

The new term $@(x, y)$ should be read 'the output of x is available as input a in y'.

► **Question 5**. What are the normal forms and what do they mean in circuit concepts?

► **Question 6**. Write the *NandC*-term corresponding to the following circuit below to the left and verify that it implements the 'exclusive or' function with truth table to the right:



x	y	z
0	0	0
0	1	1
1	0	1
1	1	0

(xor) (14)

► **Question 7**. Show that *NandC* is SN.

► **Question 8**. Show that *NandC* is complete.

One application is to find a way to measure the *speed* of circuits in the form of the *delay* from the inputs are stable until the output is stable. We'll assume that all gates use one time unit to stabilise their output after their inputs are stable and that wires have no delay, so the three circuits we have investigated so far have delay 1 (inverter), 2 (and), and 3 (xor).

► **Question 9**. Design a reduction strategy for one of the systems such that the number of strategy steps that it uses corresponds to the delay of 'real' circuits. Verify your system by checking for the three circuits above. *Hints*: Think about what properties of a circuit this depends on and that 'many step strategies' use fewer steps than ordinary reduction.

Another application is to measure the *power consumption* of circuits. We will simplify the problem by asuming that only gates that *change state* use any power.

► **Question 10**. Devise a method to measure the power consumption of circuits. *Hint*: It is alright to change the rewrite system to represent additional information.

► **Question 11 (difficult)**. Discuss how one might define a rewrite system that describes feed-back in circuits, and how such circuits correspond to simple *Nand*-circuits?

End of the exercises. © 1994 Kristoffer H. Rose (solutions available).